

In re Patent Application of:  
MAZZONI ET AL.  
Serial No. 10/088,387  
Filing Date: July 16, 2002

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**REMARKS**

The Examiner is thanked for the thorough examination of the present application, and for correctly indicating the allowability of the subject matter of Claims 6-10, 14-19, and 22-24. In view of the arguments presented in detail below, it is submitted that all of the claims are patentable.

**I. The Claimed Invention**

The present invention is directed to a device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates. As recited in independent Claim 4, for example, the device includes a channel coding/decoding stage comprising an interleaver, a deinterleaver, and a memory. More particularly, the memory has a minimum size based upon a maximum bit rate of the group of predetermined bit rates and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver. Moreover, a size of each of the first and second memory spaces is set as a function of the bit rate actually processed by the device. Independent Claim 13 is directed to a related device, and independent Claim 20 is directed to a related method.

**II. The Claims Are Patentable**

The Examiner rejected independent Claims 4, 13, and 20 based upon Djokvic et al. (U.S. Patent No. 6,956,872) in view of

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Berlekamp et al. (U.S. Patent No. 4,559,625). Djokovic is directed to system for encoding DSL information streams having different latencies. The Examiner correctly acknowledges that this patent fails to teach a first memory space assigned to the interleaver and a second memory space assigned to the de-interleaver, sizes of which each are set as a function of the bit rate processed by the device.

Nonetheless, the Examiner contends that Berlekamp et al. provides this noted deficiency. This patent is directed to interleaving schemes for digital signals. In particular, the Examiner points to FIG. 5 and cols. 6-8 of Berlekamp et al. and states that this discloses an "interleaving system that requires only one RAM for the interleaver and one additional RAM for the deinterleaver." Office Action, at 3. Furthermore, the Examiner also points to col. 4, lines 47-49 of Berlekamp et al. which reads: "[a]ssume that the data rates are equal for writing into and reading from the interleaver (and de-interleaver)."

It is respectfully submitted that the Examiner mischaracterizes the teachings of Berlekamp et al., and thus the proposed combination of references fails to teach or fairly suggest all of the recitations of the above-noted independent claims. More particularly, none of the above-noted passages or drawing figures of Berlekamp et al. teaches or fairly suggests that a size of the interleaving and deinterleaving RAMs is set as a function of the bit rate actually processed by the device. To the contrary, Berlekamp et al. provides no indication whatsoever

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as to the size or apportionment of either the interleaver or deinterleaver RAMs. Moreover, the fact that data rates for reading/writing for the interleaver and deinterleaver are the same does not mean that their sizes are set as a function of the bit rate actually processed by the device. To hold otherwise would require the impermissible use of the claimed invention in hindsight as a template or roadmap to piece together the teachings of the prior art.

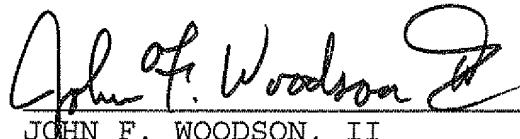
Accordingly, it is submitted that independent Claims 4, 13, and 20 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

#### CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,



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